REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claim 8 is amended to improve its form by more positively reciting method steps. The amendments are not narrowing and do not affect the claim scope.

The Examiner has objected to the phrase "said plurality of exception vector" in claims 3 and 10 under 35 U.S.C. §112, second paragraph. This typographic error has been deleted. Please withdraw the rejection.

The Examiner rejects all claims 1-15 under 35 U.S.C. §102(e) for anticipation based upon US-A-2003/0101322 (Gardner). This rejection is traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Gardner fails to satisfy this rigorous standard.

The Examiner equates Gardner's TLB register 128 in Figure 3 Gardner with the secure translation table base address register recited in claims 1 and 8. But they are not the same. As explained in paragraph [0047] of Gardner, the TLB register 128 improves performance by caching page table entries. The page table entries are the mapping data themselves. Gardner's TLB register 128 does not indicate a region of memory storing memory mapping data. Instead, TLB register 128 stores the memory mapping data itself. In contrast to this, the secure table base address register recited in claims 1 and 8 indicates "a region of memory storing secure domain

memory mapping data defining how virtual addresses are translated to physical addresses within said secure domain." For the Examiner's application of Gardner to be consistent, the TLB 128 would have to store *a pointer to the page table data* and not the page table data itself. But Gardner does not describe the former.

Claims 1 and 8 also recite both a non-secure translation table base address register and a secure translation table base address register. The TLB register 128 of Gardner does not provide even one translation table base address register, as just explained, let alone the two translation table base address registers recited in the claims.

The inventors' claimed approach to security is both necessary and advantageous. For example, to ensure sufficient security so that secure data of one application cannot be accessed by other unauthorized applications, the way in which a processing system maps virtual addresses to physical addresses must be carefully controlled in relation to a secure domain and a non-secure domain. And from a performance standpoint, switching between the secure domain and the non-secure domain should be performed quickly. These needs are met using separate translation table base address registers for the secure domain and the non-secure domain. Each register points to its own set of address translation defining data. When a virtual to physical address must be translated, the appropriate one of the translation table base address registers for the current domain can be accessed to identify the correct location for the translation data needed and then that translation data may be accessed. Consequently, these sets of data are kept separate and secure. Moreover, switching from one to the other can be rapidly done as explained in the specification.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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